

ASIC Design Flow

FIG. 1

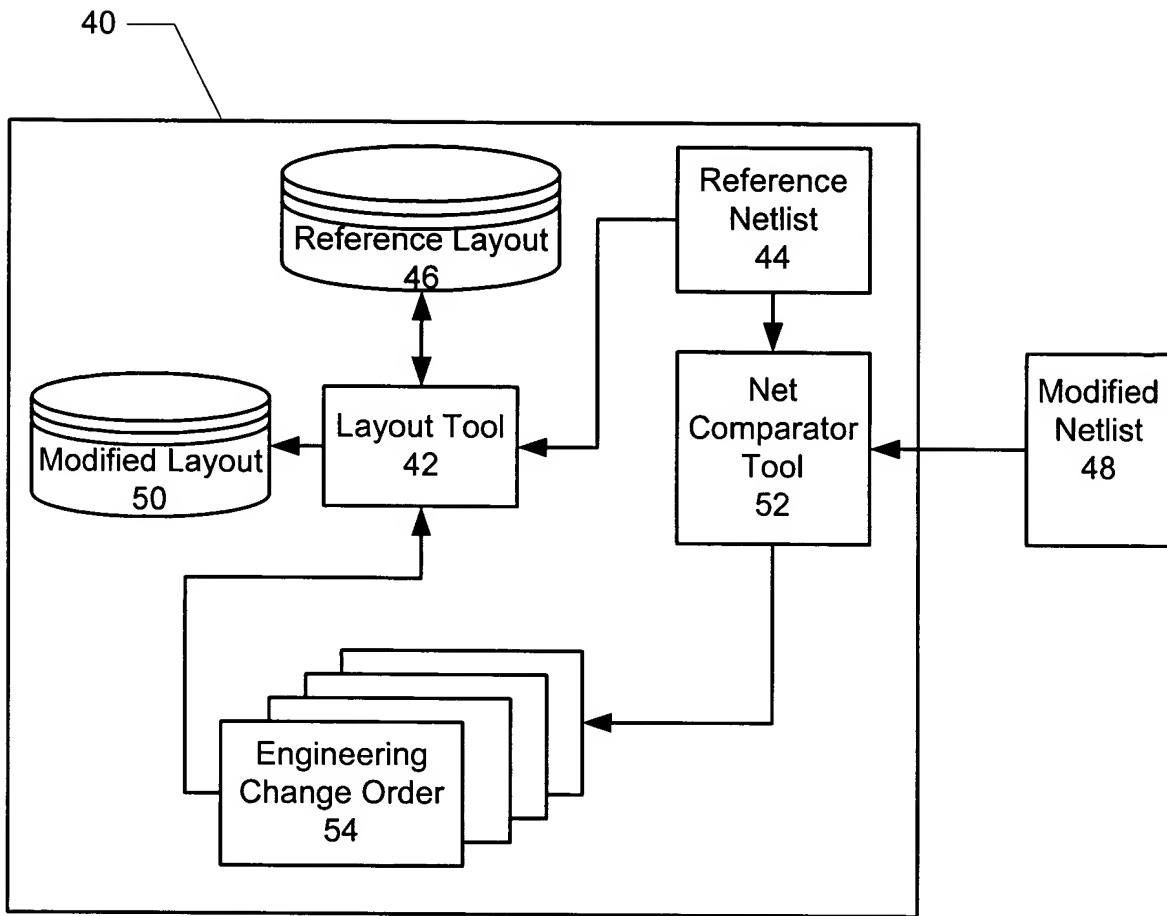


FIG. 2

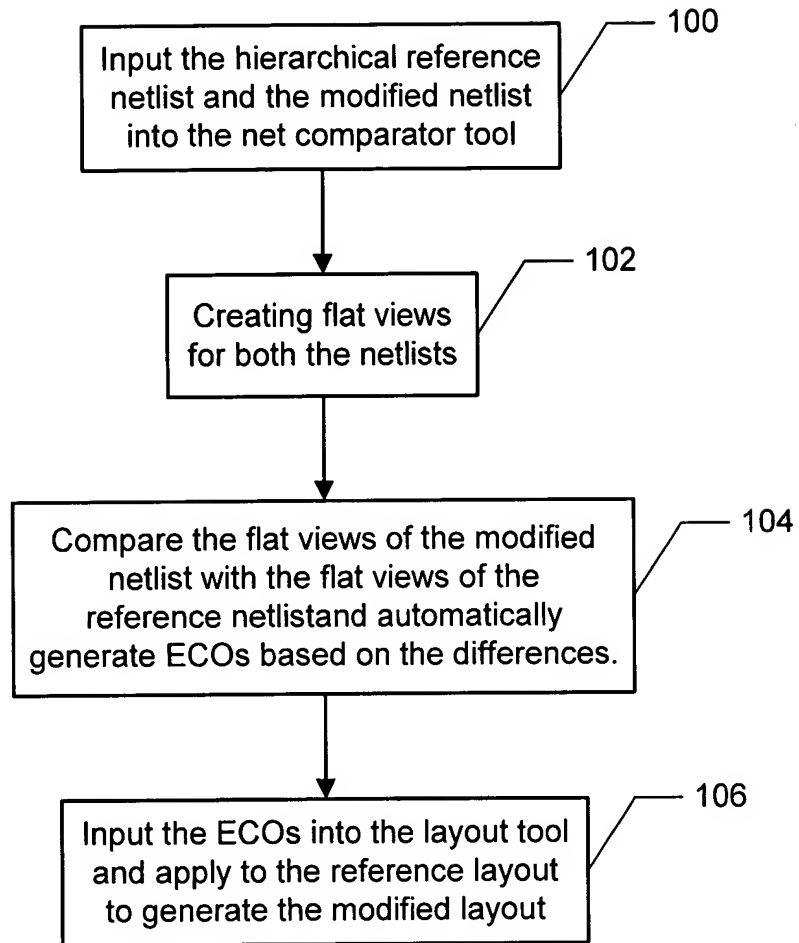


FIG. 3

44

```
// Sample hierarchical Reference Netlist.  
  
module foo(A1,A2,Z);  
  input A1,A2;  
  output Z;  
  wire n1,n2;  
  
  AND2AFP u1(.A(A1),.B(A2),.Z(n1));  
  
  N1AFP u2(.A(n1),.Z(n2));  
  
  BUFAFP u3(.A(n2));  
  
  hier_module u4(n2,Z);  
  
endmodule  
  
module hier_module(B,Z);  
  input B;  
  output Z;  
  
  FD1QAFP u5(.D(B),.Q(Z));  
  
endmodule
```

FIG. 4A

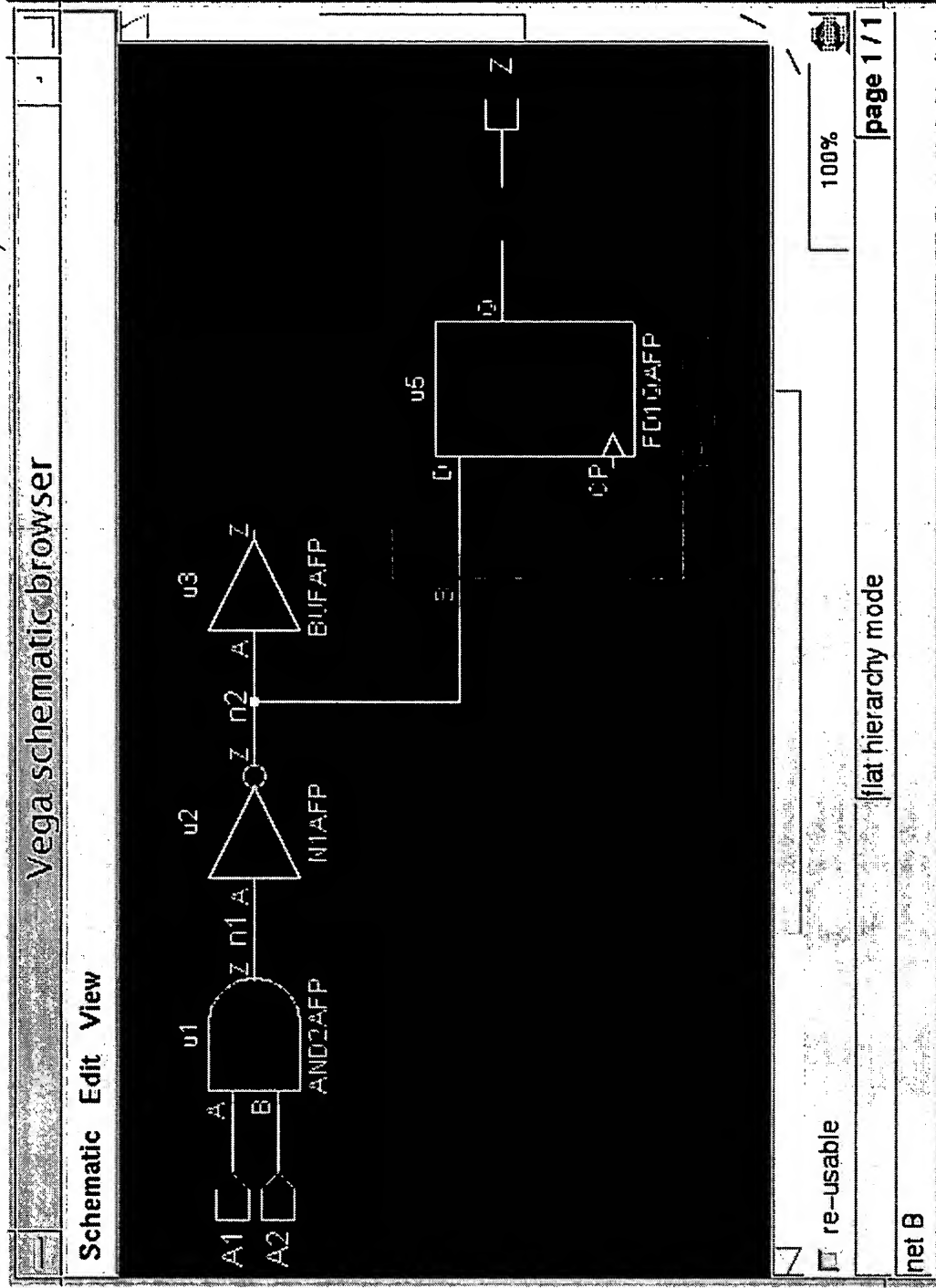


FIG. 4B

48

```
// Sample hierarchical Modified Netlist

module foo(A1,A2,Z);

input A1,A2;
output Z;

wire n1;

// AND2AFP cell-type changed by the designer.
// to do some logic restructuring.
ND2AFP u1(.A(A1),.B(A2),.Z(n1));

BUFAFP u3(.A(n1));

// The herarchical module.
hier_module u4(n1,Z);

endmodule

module hier_module(B,Z);
input B;
output Z;

// New net-added by the user.
wire n_n;

// New buffer added by the user.
BUFAFP u_n(.A(B),.Z(n_n));

// Flop type changed to a stronger one.
FD1QCFP u5(.D(n_n),.Q(Z));

endmodule
```

FIG. 5A

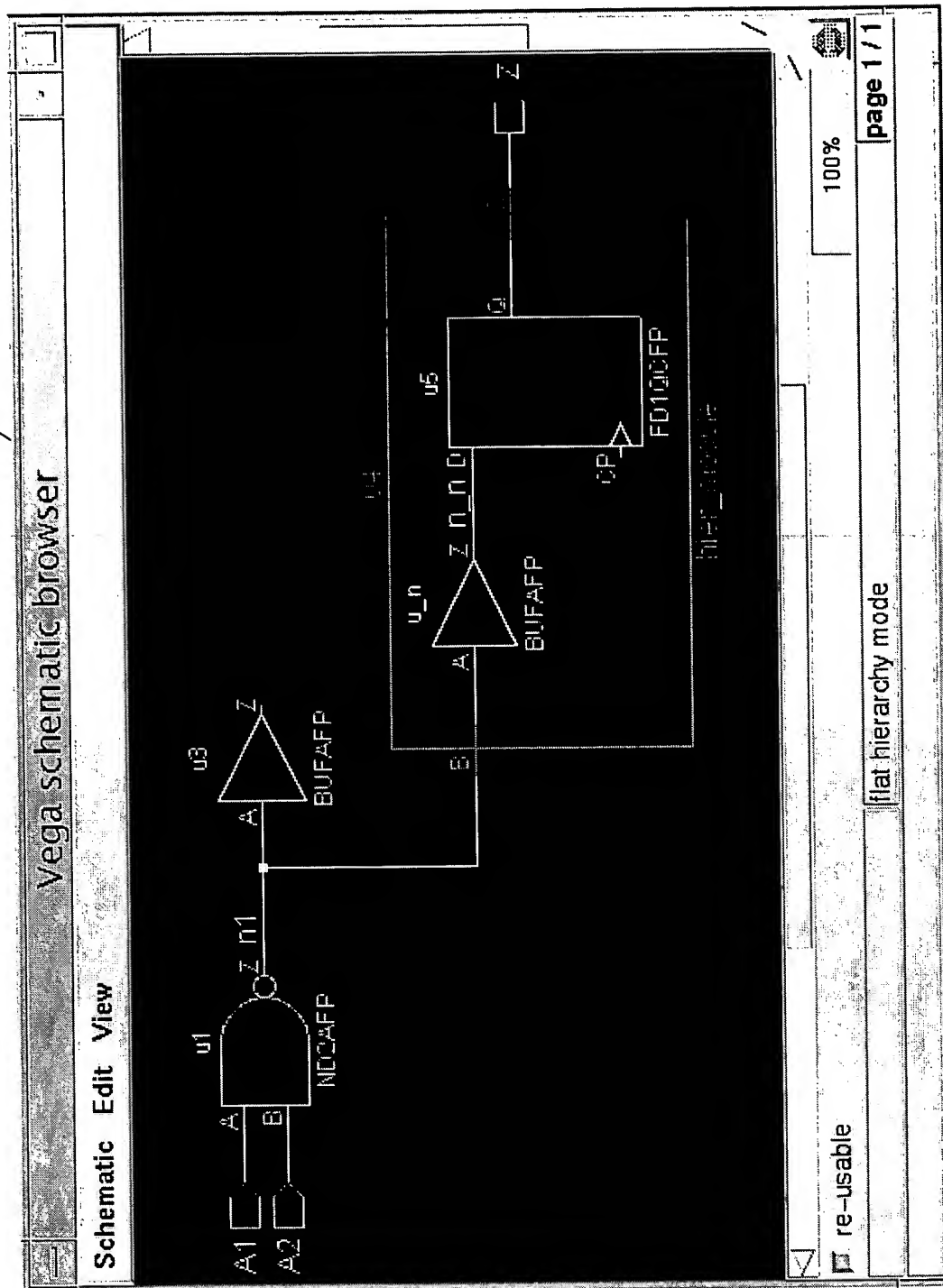


FIG. 5B